CLAIMS

Having thus described our invention, what we claim as new, and desire to secure by Letter Patent is:

1. A SRAM cell fabricated in SSOI (selective silicon on insulator) comprising:

cross coupled pnp pull-up devices P1, P2 having sources, drains and gates and npn pull-down devices N1, N2 having sources, drains and gates, with the P1, P2 devices being connected to a power supply and the N1, N2 devices being connected to a ground;

a first passgate NL coupled between a first bitline and the junction of devices P1 and N1, with its gate coupled to a wordline, and a second passgate NR coupled between a second bitline and the junction of devices P2 and N2, with its gate coupled to the wordline, and the passgates having sources, drains and gates:

wherein each of the pull-up devices P1, P2, the pull-down devices N1, N2, and the first and second passgates NL, NR are fabricated with their sources, drains and gates being selectively provided with SOI or being fabricated over bulk silicon without SOI.

2. The SRAM cell of claim 1, wherein the drains of the pull-up devices P1 and P2 and the pull-down devices N1 and N2 are provided with selective SOI to reduce the capacitance of the drains to allow the potential of the drains to be moved/changed faster to increase the circuit speed.

3. The SRAM cell of claim 2, wherein the voltage supply, source sides of the pull-up devices P1 and P2 and the ground, source sides of the pull-down devices N1 and N2 are fabricated over bulk silicon without SOI.

4. The SRAM cell of claim 3, wherein channels under the gates of the pull-up devices P1 and P2 are biased/touched to VDD of an underlying N well and are fabricated over bulk silicon without SOI.

5. The SRAM cell of claim 4, wherein channels under the gates of the pull-down devices N1 and N2 are biased/touched to ground of an underlying P well and are fabricated over bulk silicon without SOI.

6. The SRAM cell of claim 1, wherein each of the pull-up devices P1, P2, the pull-down devices N1, N2, and the first and second passgates NL, NR have bodies that are biased by being biased/coupled to the voltage supply or to ground through an underlying N well or an underlying P well.

7. The SRAM cell of claim 1, wherein the sources of the pull-up devices P1 and P2 are coupled to the voltage supply, the sources of the pull-down devices N1 and N2 are coupled to ground, and the gates of the passgate devices NL and NR are biased/coupled to ground through an underlying P well.

8. The SRAM cell of claim 1, wherein the drains and the sources of the passgates NL and NR are provided with selective SOI to reduce the capacitance of the drains and sources to allow the potential of the drains and sources to be moved/changed faster to increase the circuit speed.

9. The SRAM cell of claim 1, wherein channels under the gates of the passgates NL and NR are biased/touched to ground of an underlying P well.

10. The SRAM cell of claim 5, fabricated with selectively placed buried oxide under the drains of the pull-up devices P1 and P2, the drains of the pull-down devices N1 and N2, and the sources and drains of the passgate devices NL and NR.